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Aeris DAC: Genesis and Innovations

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Technical Features

IsoSync ECS: A jitter removal system based upon an asynchronous buffer, voltage controlled crystal oscillators (VCO), and a 24-bit D/A converter – all under the precise control of FPGA (Field Programmable Gate Array) running proprietary algorithms. IsoSync ECS results in the reduction of total jitter to less than 10 picoseconds RMS from any input – USB, TOSLINK, and SPDIF.

Multi-Stage Isolated Power Supply: Main power supplies are isolated inside an external machined aluminum chassis. Eleven precision high-speed regulators provide low impedance and low noise "point of load" DC current to all analog and digital circuits. – What part of the power supply is isolated? Unregulated.

Isolated Audio and Digital Circuitry: Left and right channel audio output circuits, digital processing, and D/A conversion circuits are isolated within individual milled aluminum pockets, resulting in exceptional EMI shielding, and thermal stabilization.

FPGA-driven Volume Control with Overdrive: Wide range level control of outputs permit direct connection to power amplifiers exceeding dynamic properties of traditional active preamplifiers. – Tight.

USB Driver-Free Operation: The USB interface requires no additional drivers to install or maintain/update. The USB interface is plug-n-play with all operating systems, including PC, Mac, or Linux.

6-Layer Printed Circuit Boards (PCB): Our implementation of the circuit board provides extremely low impedance ground and power distribution for remarkably low digital noise contamination.

High-Precision Surface Mount Components: Extensive use of lead (Pb)-free, low temperature coefficient, active and passive surface-mount components results in significantly smaller loop areas, reduced circuit capacitance and inductance, and introduces less noise than conventional leaded components.

Transformer Coupling: Transformer coupled balanced XLR line outputs and BNC/SPDIF input provide outstanding output common-mode noise rejection, eliminate potential ground loops, and ensure compatibility with other equipment.

Machined Aluminum Chassis: Precision-machined chassis milled from a solid block of aircraft grade 6061-T6 aluminum, provides exceptional thermal stability, RFI/EMI shielding, and resonance control.

Output Connectors: Rhodium / Teflon Cardas output connectors for both balanced and unbalanced outputs preserve maximum audio signal integrity.

IsoSync ECS (Error Correction System)

The Aeris accepts digital data synchronously with the source device, and stores information temporarily in a small asynchronous buffer, capable of storing 44 data samples (x2 and x4 for higher rates), equivalent to 1 millisecond of audio.

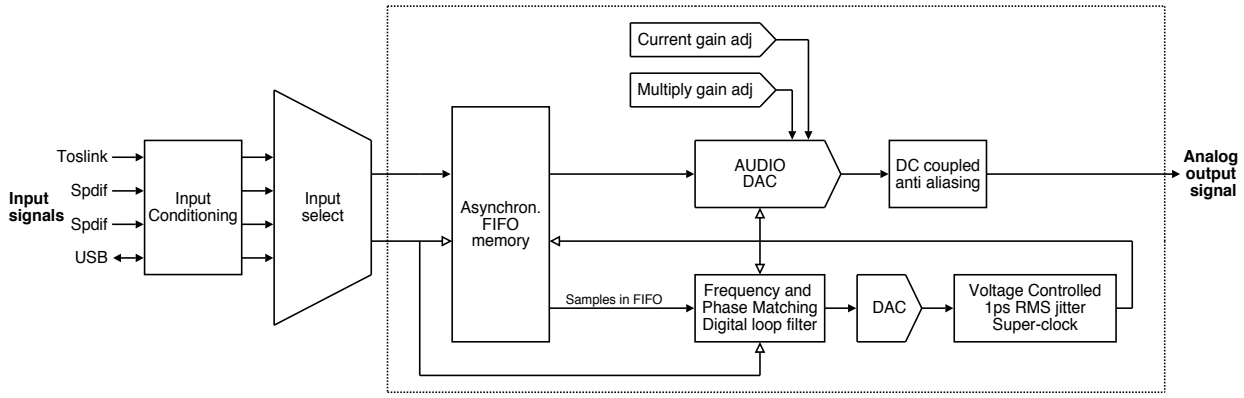

Fig. 1: Isolated Synchronous Error Correction System (IsoSync ECS)

The data buffer operates under completely separate and independent clock domains for input and output. In other words, there exists one clock running at the input of the buffer, and a second clock dedicated to the buffer's output. The input clock is derived from the source sample rate, using standard technology and standard ICs. Conversely, the output clock is generated with from a proprietary clocking system.

The two clocks are completely isolated from each other, and not connected in any way. The clocks are, however, running at identical rates, and therefore can be considered both isolated and synchronous.

Sources of Jitter

Jitter arises from clock pulses not having an infinite rise time. Rather, the pulses exhibit a sloped edge. The electronics that receive and detect this edge have a trigger voltage at a defined level. When the signal is polluted by a magnetic field, an electric field, power supply noise, or ground bounce, the sloped edge timing is offset with respect to the original trigger voltage at the input point. This effect generates a minute amount of shift in the timing of the received clock signal. This shift in timing is what we call jitter. There are many types of jitter, but we will treat jitter as a general term for the purposes of this paper.

A theoretical solution would be to generate a clock edge with infinite rise time. This is, however neither practical nor possible, as it would put a demand for extreme high

bandwidth on cabling with associated impedance matching issues. In the real world, impedance matching on cables and terminations are not perfect over all frequencies, a reflection of the clock edge will always be generated at cables terminations. The reflection will distort trigger level and thus generate jitter.

The digital input receiver is another common source of jitter. The receiver recovers a system clock from the incoming data rate using a PLL (Phase Locked Loop). PLLs must employ a filter and control voltage for a Voltage Controlled Oscillator (VCO). The control voltage must be completely free from noise, and absolutely stable, for the PLL to perform without jitter.

There are additional sources of jitter in a system. Source components and cabling for example, both generate significant amounts of jitter. Moreover, digital interface receivers have a PLL that also generates jitter of its own. A USB data stream (computer audio sources) also add their own characteristic jitter to a signal.

Automatic IsoSync ECS Sampling and Upsampling

IsoSync ECS adapts and operates automatically with full 24-bit resolution on all standard sampling rates:

- 44.1 KHz
- 48 KHz
- 88.2 KHz
- 96 KHz
- 176.4 KHz
- 192 KHz

Incoming data is routed bit-perfect to the DAC chip, where it is normalized by selective up-sampling:

- Single rate 44.1 KHz material is converted to 352.8 KHz by 8x upsampling.
- Single rate 48 KHz material is converted to 384 KHz by 8x upsampling.
- Double rate 88.2 KHz material is converted to 352.8 KHz by 4x upsampling.
- Double rate 96 KHz material is converted to 384 KHz by 4x upsampling.
- Quad rate 176.4 KHz material is upsampled to 352.8 by 2x upsampling.
- Quad rate 192 KHz material is converted to 384 KHz by 2x upsampling.

In other words, single rates are upsampled 8x, double rates are upsampled 4x, and quad rates are upsampled 2x.

The Aeris upsampling process reduces the staircase step size of the current out of the DAC chip, and any related aliasing. It achieves the smoothest possible DAC current output. This is particularly important because large current source changes that exceed certain

thresholds could cause circuitry down the chain to exceed slew rate capabilities, which in turn would generate various types of analog distortion.

IsoSync ECS Functional Description

Data is received by the Aeris using standard adaptive mode USB, or digital interface receivers like SPDIF via 75 ohm BNC and TOSLINK inputs. A certain amount of initial jitter is assumed. The initial focus is to register the audio data in a bit-perfect format, rather than focusing on jitter. Bit-perfect data is written to the IsoSync ECS buffer synchronously to the input clock. When the buffer is filled with 1 millisecond worth of data, an output process commences with bit-perfect reading on the output side of the buffer, using the isolated clock within the Aeris. The isolated clock is generated by a high performance VCXO (Voltage Controlled Crystal Oscillator). The control voltage for the VCXO originates from a low noise voltage output DAC, whose numerical value comes from a digital loop filter that monitors the amount of data in the buffer, and the phase relationship between the incoming clock and the VCXO clock.

The IsoSync ECS hardware has been implemented with the following component parts:

1. A Digital interface receiver
2. An FPGA-based (Field Programmable Gate Array) Asynchronous FIFO (First in, First out) Buffer with separate clock for input and output
3. A digital loop filter. (FPGA based)
4. A dual 16-bit DAC merged to create a single 19-bit digital to analog converter
5. Two VCXOs (Voltage Controlled Crystal Oscillator), one for 44.1kHz and the other for 48kHz based sample rates
6. A clock buffer for driving both FPGA and DAC chips

The resulting clock signal output of the VCXO has an extraordinarily low jitter spectrum below 10 pico-seconds rms. (Summarize)

Dual Control Modes for the VCXO

Seek-lock mode: The Aeris activates a seek-lock mode and matches the incoming sample rate. This process takes approximately one-half second. When the sample rates are matched, the digital loop filter returns automatically to the lock-mode.

Lock-mode: In lock-mode, the rate of change on the VCXO voltage is extremely slow. Phase drift is monitored constantly, and VCXO voltage is adjusted when the drift falls outside a specified tolerance. The voltage is adjusted only if the phase of an incoming or outgoing sample has drifted out of range. The drift rate and direction is constantly monitored, and the voltage level change going to the VCXO is parameterized. This optimizes the amount of change and ensures the longest possible time interval between updates to the VCXO. Whenever the phase drift is measured as $2/128^{th}$ (or greater) of a

sample, or it is predicted that drift is too fast, the VCXO is updated. Typically, VCXO voltage is adjusted only 4 to 6 times per hour.

The system features a 19-bit resolution with a pull range of +/- 100 ppm (parts per million). This corresponds to 0.000381 ppm per increment, or in other words, a frequency change of 8.6 millihertz on a clock rate of 22.5792 MHz. The accuracy of frequency stabilization is staggeringly precise.

Such exceedingly small corrections performed on the control voltage imply that the VCXO is essentially free-running, or is at least operating under free-running specifications.

Compared to typical Phase Locked Loop (PLL) systems, the Aeris implementation generates significantly less jitter from the controller itself. One of our design goals was to eliminate residual problems as close as possible to the DAC chip signal source.

After conversion to analog some residual current shifts may remain out of tolerance. Such swings would result in exceeding op-amp slew rate boundaries, with the undesirable consequences mentioned above. Therefore, we have implemented output filters on the DAC chip current output pins thus eliminating the problem.

Bit-Perfect Preservation

IsoSync ECS is a highly attractive approach to jitter elimination because it is capable of preserving the source signal in a bit-perfect form while completely restoring the timing information contained in the original recording. Virtually all timing errors introduced and accumulated from all sources are removed *before* entering the DAC chip. Therefore, the performance characteristics are exceptional from all Aeris inputs**.**

BNC S/PDIF and Transformer Coupling

The Aeris supports a coaxial BNC connection due to the fact that the BNC connection guarantees that the input impedance remains stable at a nominal 75 ohms. In addition, both the Aeris BNC S/PDIF digital inputs achieve galvanic isolation of the incoming signal through transformer coupling. Total galvanic isolation is achieved by implementing transformer coupling also at the XLR balanced analog outputs.

The Aeris has implemented transformer coupling on the BNC S/PDIF inputs through the PE65812NL by Pulse Engineering Inc, a transformer optimized for digital signal transmission. This surface-mount part was selected because its wide bandwidth supports a sample rate up to 192 KHz.

Limitations of the AES/EBU Connection

AES/EBU inputs (XLR) were not included on the Aeris DAC because the AES/EBU connector itself is not typically rated for the required 110 ohm characteristic impedance.

Only a 75 ohm industry standard BNC interface connection on both the source, cable, and load will guarantee a true high performance, low jitter, high bandwidth, transfer of data – only achievable without cable reflections.

Analog and digital signals make entirely different demands on cables and their respective connectors. Analog audio is a relatively low frequency (0-200htz), low impedance to high impedance, connection requiring extreme noise rejection and therefore benefits greatly from a balanced connection. Digital is a high frequency (reaching well into the MHz region) connection that requires exact impedance matching between source, load, and interconnect to eliminate signal reflections.

The BNC connection is a decades old industry standard that is guaranteed to meet the demanding requirements of digital data transmission. The AES/EBU format, incorporating XLR connectors on both chassis and cables is generally not guaranteed to provide a true 110 ohm impedance at the source, load, and interconnects. It would be too easy for a consumer to use a standard XLR balanced audio cable with the AES/EBU XLR connector into a D to A converter, seriously compromising its performance.

If the source component (digital player) has an AES/EBU XLR output connector, a matching transformer/adaptor[1], which converts the AES/EBU XRL balanced connector to a BNC 75 ohm connector, can be used at the source component output. This will allow use of virtually any length of 75 ohm coaxial cable and guarantee that the interconnection to the Aeris will offer a full bandwidth data transfer with minimal signal reflections and resultant jitter generation.

Limitations of Asynchronous USB Interfaces

IsoSync ECS overcomes one of the major limitations of asynchronous interfaces between a DAC and data source such as a computer. In most cases, asynchronous interconnections require the DAC to operate as the host and the computer to operate as the slave, which can require the installation of drivers. The Aeris does not require the installation of any drivers and can operate with any operating system.

Any USB source should be ideally located as far as possible from the rest of the audio system to minimize the impact of radiated RF and EMI. The Aeris SP/DIF inputs utilizing the BNC 75 Ohm connectors guarantees that there is no practical distance limitation between a digital source and the Aeris. The USB cable has much more restrictive length limitations – between 3 and 5 meters maximum.

[1] Canare BCJ-XJ-TRB 110 Ohm to 75 Ohm Digital Audio Impedance Transformer can be ordered from B&H Photo.

USB Challenges And Solutions

The Aeris USB input interface is based on the Texas Instruments TA1020B receiver. For any source connected to the Aeris via USB, jitter removal is performed in two separate steps: the USB interface subsystem provides initial jitter removal of the incoming data, then data is passed to the FPGA for near total jitter removal via IsoSync ECS processing.

During the design of the Aeris USB interface circuitry, the project team led by Ask Bojesen, discovered that the Texas Instruments TA1020B USB interface Chip PLL implementation suffered from several numerical bugs that impacted the jitter performance, and therefore the quality of the incoming data stream. The project team worked with a member of the original TI team to troubleshoot and remedy these issues. This resulted in vastly lower initial jitter values from the USB interface and established a much lower baseline for jitter elimination in the downstream IsoSync ECS FPGA based subsystem.

High Performance TOSLINK

IsoSync ECS is designed to operate maximally on all Aeris inputs, including TOSLINK. IsoSync ECS greatly reduces any jitter introduced by the jitter-prone TOSLINK electro-optical circuits, and is so effective that it transforms TOSLINK into a very high performance data input.

DAC-based Volume Control

One of our primary design goals was to create a simple and short audio signal path. By implementing the Aeris volume control in the DAC chip, we were able to omit several discrete analog components that would have lengthened the signal path, and could have introduced distortion. We selected a DAC chip that is one of the only available that supports an adjustable current reference input range that is wide and stable enough for a true high-end volume control.

The Aeris volume control operates over a full 70dB range, with a step resolution of 1dB. The volume control is neither purely analog nor purely digital. Rather, the volume control operates by varying the reference current in the DAC chip, over a 32dB range. We have determined that within that 32dB range, the DAC chip operates linearly. Within this range no mutual left/right channel drifts can be nearly immeasurable.

In order to extend the usable gain range to a total of 70dB, we have implemented an internal multiplier on the DAC chip. In theory, this multiplicative technique may lose some low-order bits – typically 1-bit per 6dB of attenuation. However, when operating with the 24-bit resolution, the loss remains below the S/N ratio of 117dB (A-weighted at 48 KHz).

Creating the Volume Control Current Reference

The current reference for the DAC chip is generated by implementing a low-noise Linear Technology D2A (digital to analog) converter. The D2A voltage reference is a buffered version of the voltage found on the DAC chip current reference pin. The D2A drives the other end of a low noise thin film resistor, and modulates the DC current emerging from the DAC chip current reference pin. This yields an excellent linear stepped control of volume with 1dB resolution. The steps are matched to the digital domain step size.

Benefit of the Volume Overdrive Feature

In the early days of digital recordings, recording engineers were not able to calibrate their recording equipment to the maximum reference dynamics. Instead, they prevented unexpected clipping by making conservative estimates. As a result, this drastic approach to clipping prevention yielded CD recordings that could lose up to 50% of the available dynamic range. Even today, some conservative engineers limit the dynamic range.

On those recordings that are not utilizing the full digital dynamic range, the Aeris "overdrive" gain allows an expansion of the incoming dynamics to harvest the complete dynamic capabilities of the DAC chip without excessive clipping.

When the volume level is increased beyond 0dB gain into this overdrive region, the LED volume indicator starts blinking. In overdrive mode, the volume indicator ranges from +1 to +20dB.

Direct Driving an Amplifier

Most current DAC designs lack enough positive digital gain to drive higher output levels. The Aeris can supply a high enough output level such that it can be used to drive a power amplifier directly.

Benefits of a Single DAC Chip Design

We made a deliberate decision to base the Aeris design on one single DAC chip, used in stereo mode, rather than one DAC chip per channel. The single chip design is inherently free from any inter-DAC chip delay. A delay of up to 10 nanoseconds (10,000 picoseconds) has been measured when using multiple DAC chips in parallel. The Master Clock reference to the Aeris DAC chip is below 10 picoseconds RMS with un-measurable channel-to-channel delay.

Multi-Stage Isolated Power Supplies and Regulation

The Aeris is powered by two separate low noise, passive power factor corrected, switch mode power supplies (SMPS) – one for analog and one for digital. Both are housed in a single machined external enclosure for maximum mechanical and EMI/RFI isolation.

A long life solid-state relay provides low in-rush current, zero-crossing, AC mains power switching from standby to power-on. This circuitry allows for an AC mains standby power of less than one watt.

This power supply provides fully regulated DC output voltages and is immune to AC mains brownouts, surges, and mains born noise. The Aeris will operate over a range of 85 to 265 volts.

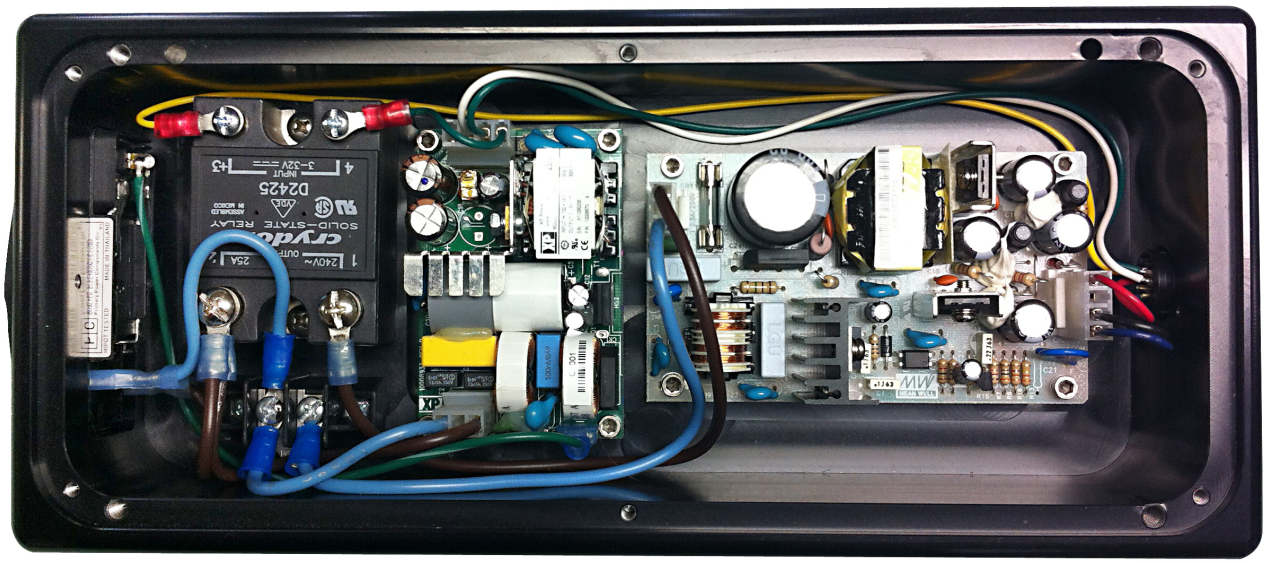

Fig. 2: Machined aluminum external power supply

Regulated DC voltages from the power supply are further regulated by 11 precision analog high-speed regulators which provide low impedance and low noise "point-of-load" DC current to all analog and digital circuitry. We selected recently developed linear, ultra-low noise (15 microvolts), low-drop regulators that provide a power supply rejection ratio (PSRR) of 72dB at 120Hz and 52dB at 400kHz.

As a result of this hybrid power supply configuration, any theoretical performance advantage of purely linear power supplies over SMPS becomes irrelevant.

Post-regulated Power Rails

By adding the power supply rejection ratio (PSRR) to the op-amp's PSRR, we obtain an extraordinarily high combined value above a theoretical 200dB (wide-band), which is well below any measurable and audible threshold. As a result, the Aeris is essentially free from any intrusion of external power supply conducted noise into the final analog signal. An additional benefit is a left/right cross talk specification of greater than -120dB.

Both positive and the negative analog power rails are distributed on their own PCB power planes with an area of 60 x 60 mm each. Each channel has its own regulators. The analog section has six regulators total – two of which are dedicated to the DAC chip.

Benefits of the LME49990 and Ultra Low Total Harmonic Distortion

The quality of the analog and digital sections of any DAC are equally important. An extremely accurate, stable, and linear digital section requires that the corresponding analog sections of the device be extremely low noise, so as not to destroy the purity of the signal just decoded.

For example, 24 bits of digital resolution convert to a total harmonic distortion of 0.0006% in the analog domain. 16 bits convert to a THD of 0.0016%. Even the latter values can be difficult to achieve throughout the entire audio frequency range at line levels in a preamplifier.

For this very reason the Aeris design utilizes the LME49990, the latest National Semiconductors IC capable of textbook specification for noise, distortion, output impedance, and all other classical measurements used in audio circuits. The LME49990 is used for current conversion, post DAC filtering, and output buffers in the Aeris.

The LME49990 op-amp was selected for its remarkable technical specifications, which include:

- A low noise of 0.9 nanovolts per square root Hz
- A low THD plus noise of 0.00001%
- A high Common Mode Rejection Ratio (CMRR) of 137dB
- A high Power Supply Rejection Ratio (PSRR) of 144dB

LME49990 is designed specifically for ultra-high end audio applications. Its technical specifications are so low that actual measurements could not be made unless the device parameters were multiplied by 10x.

6-layer FR4 PCB Design

Any analog circuitry is potentially very sensitive to noise emanated by nearby digital logic. So conducted noise from digital circuitry switching must be sufficiently attenuated through high power supply rejection ratio, intelligent printed circuit board (PCB) design, grounding methods, and shielding. The goal is to achieve a pure DC voltage source for all circuitry at all frequencies. In the Aeris, excellent noise rejection is obtained by incorporating a 6-layer circuit board, for a total S/N ratio of 200dB.

In the Aeris 6-layer PCB, two complete layers are dedicated to ground. The clock signal is isolated from the signal path by these two grounding layers. Two layers are dedicated to

power distribution, and two layers are dedicated to signal distribution. As a result, the clock signal cannot be contaminated by the audio signal.

FPGA and digital interface (digital section), digital to analog converter (digital to analog section), left analog and right analog (analog section) are all segregated.

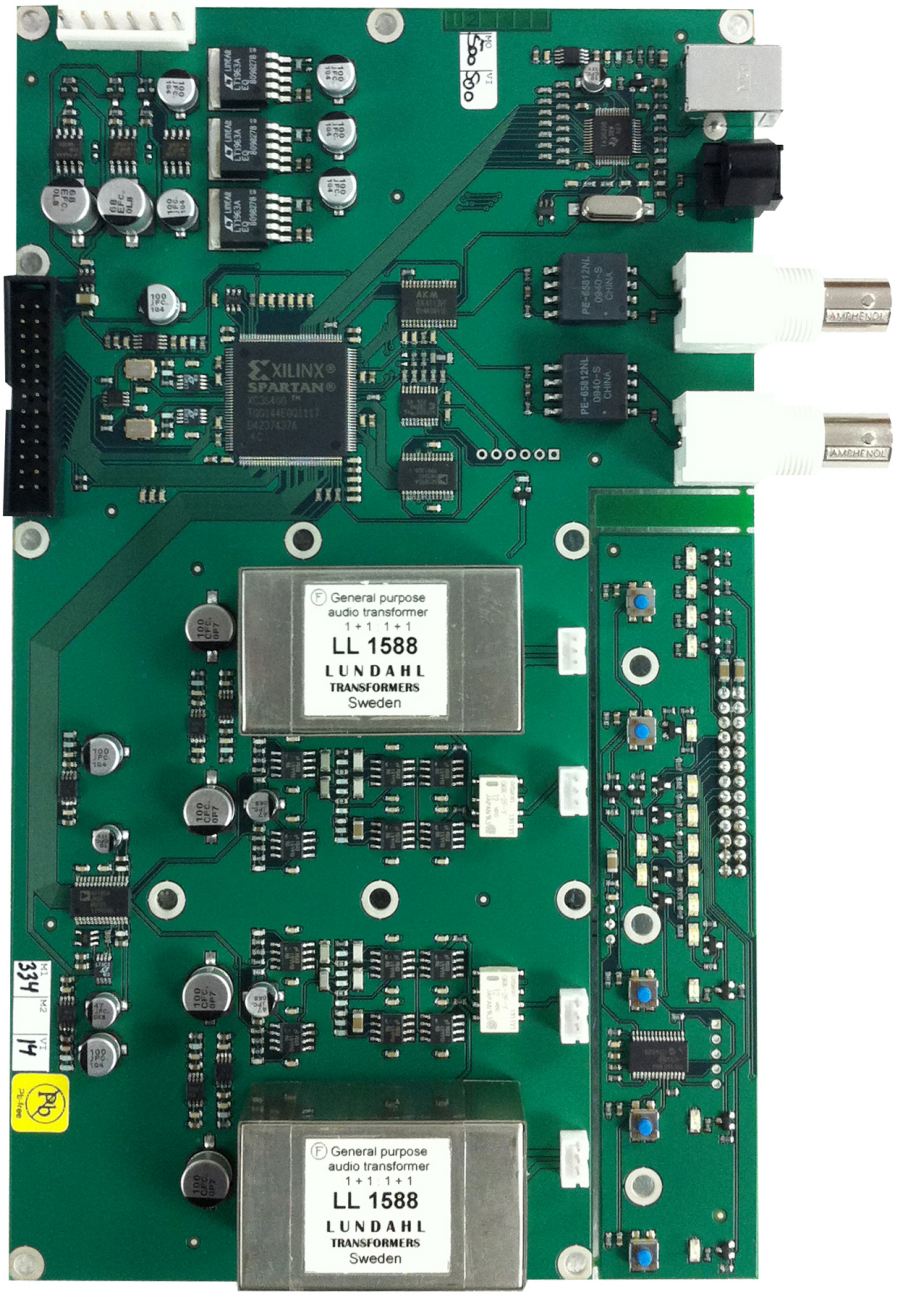

Fig. 3: 6-layer FR4 PCB design

The ground layer is complete over the entire board to keep all current loops intact and as small as possible. High-speed currents will try to find the path of least inductance and resistance. This means the ground layer under a signal trace needs to be intact, or else the return current in the ground layer would seek a path away from its trace. The resulting detour would generate unwanted EMI fields and ground bounce. However, as all signals refer to the ground plane, this must remain absolutely free from ground bounce.

For instance, the DAC chip and its support circuitry reside within their own 25mm by 125 mm surface area. The analog and digital power supplies supporting the DAC chip are taken from separate post-regulating power regulators. These regulators exhibit an extremely low noise level of 15 microvolts rms. They are distributed over the two separate PCB layer areas, one for the analog supply to the DAC chip, and one for the digital supply to the DAC chip. Using a large area for conduction, the PCB layer provides an extremely low impedance. The power distribution layers also act as distributed high-speed capacitors that decouple noise into the ground layers. By design, we use the PCB as another effective electrical component.

Surface-Mount Devices

All circuitry is implemented using SMD (surface mount devices). Among the many benefits of using SMD is that grounding planes and power planes are not perforated by component pins, which keep the power and grounding planes intact.

The additional benefits of SMD components is keeping loop areas as small as possible and allowing these components to be located as close as possible to corresponding ground planes. Smaller loop areas provide a high immunity from external noise (inherent shielding) and conversely reduce radiation from respective conductors.

Capacitor Considerations

The Aeris analog section incorporates NP0-type high quality ceramic SMD capacitors, which are the best capacitors available in SMD. Capacitors in the signal path operate only in the extreme low or extreme high frequencies, below 1Hz and above 70kHz. As a result, no capacitors in the signal path ever affect the audible frequency range.

Resistor Considerations

All resistors in the Aeris are thin-film, 0.1% tolerance, 0603 SMD type, approximately 1mm wide by 2mm long. These exhibit as much as 20db less noise than conventional resistors. Shot-noise (a particular type of electrical noise) is generated by electrons that resist changing quantum state. Electrons maintain their binding to an atom until they have absorbed enough energy to pull free of their orbit. This phenomena is somewhat like pulling an elastic band until it snaps. Shot-noise prone areas in the resistive material are created by “burning” from laser trimming in the manufacturing process. As thin-film

"burns" more cleanly than thick film, less shot-noise is produced. Furthermore, noise in thin-film resistors is less voltage-dependent than in conventional resistors.

Transformer Coupling

The Aeris incorporates Swedish made Lundahl output transformers on both balanced XLR right and left channel outputs. These transformers provide the ideal buffer between the internal output stage circuitry and the outside world. Besides providing a true balanced output configuration, with a very high output common mode rejection ratio, the transformers provide true galvanic ground isolation. A virtually infinite impedance between any ground noise and signal is achieved, as well as the buffering – or fire wall – between the Aeris output circuitry, and any RF or EMI which could enter the output connectors.

Piezo-electric Effect Prevention

The piezo-electric effect is the generation of electrical noise resulting from the microscopic bending or flexing of electrical devices in any circuit and external airborne and mechanical vibrations from any source. The piezo-electric effect will introduce distortion into the signal path. Capacitors and silicon devices are particularly sensitive to this effect. To minimize the this effect, the Aeris PCB is rigidly anchored at all critical points to the solid, non-resonant, virtually airtight, machined aluminum chassis.

Dual Audio Outputs

The single-ended RCA outputs are buffered and independent from the XLR outputs, which are isolated with the output transformers as mentioned above. This allows the Aeris to drive two amplifiers simultaneously and isolate the ground currents and load demands of each output.

Output Muting

Relay contacts in parallel with the signal outputs prevent unwanted noises when the Aeris power is cycled on and off. This relay grounds the output temporarily when the device is powered on or off. Because the relay is in parallel with the signal path, no signal passes through the relay when the unit is on.

Milled Chassis and Functional Isolation

The relatively high physical mass of the Aeris chassis also provides a high thermal mass, resulting in excellent thermal stability. Once a stabilized temperature is reached, the Aeris chassis resists any further thermal gradients that could induce mechanical stresses resulting in piezo-electric effect related distortions. Small pockets machined into the Aeris chassis separate different sections and minimize the amount of air that can be heated in any one section. Since air has low thermal inertia, and readily transmits heat, this segregation provides further thermal stabilization for each section.

Fig. 4: Machined aluminum chassis with isolated pockets

Specifications

Inputs	1x USB (B-type)	Accepts up to 24 bit PCM at 44.1, 48, 88.2, and 96 kHz sample rates
	1x Toslink (Optical)	Accepts up to 24 bit PCM from 11 - 192 kHz sample rates
	2x SPDIF (RCA)	Accepts up to 24 bit PCM from 11 - 192 kHz sample rates
Outputs	1 pair balanced XLR / 1 pair unbalanced RCA	7 volts RMS max output level
Volume Control	Dual-stage attenuation	70 dB range, plus 20 dB overdrive
Software/Drivers	No special drivers necessary	USB interface is plug-n-play with all operating systems, including PC, Mac, or Linux.
Clocks (2X)	20 bit dynamic range	Voltage Controlled Crystal Oscillators (VCXO), 44.1 kHz and 48 kHz < 10 picosecond RMS jitter
D/A Converter	Differential output	352.8 kHz, 24 bit
Digital Filter	Finite Impulse Response (FIR) symetrical	Flat phase and group delay
THD+N	Analogue outputs	< 0.0006%
Output Impedance	RCA / XLR	120 ohms

Biographical Information

Jeff Rowland, President, *Jeff Rowland Design Group*

Jeff Rowland's electronics career began at age of 12 with the simple yet powerful question, "How does it work?" Driven by what would become a life long passion for design, Jeff disassembled, reassembled, and redesigned radios and televisions salvaged from a local scrap yard. By high school, he had willfully transforming a childhood hobby into an intense and focused independent study.

As a high school senior, Jeff enrolled in a "work-study program" that landed him a part time job as an electronics test technician at the well known local tape recorder manufacturing plant, Ampex Corporation.

After graduating high school with a scholarship to the school of his choice. Rather than a traditional four year EE programs offered by popular universities, Jeff chose a newly chartered electronic engineering school that focused on entirely on electronic engineering. After two years of analog engineering studies DeVry Institute of Engineering Technology, Jeff returned to Ampex Corporation as an engineering assistant.

In 1975, Jeff expanded his career experience at another local engineering company, Kaman Sciences and Instrumentation, where Jeff worked on diverse projects such as precision temperature and displacement measuring systems.

Throughout these formative years, Jeff's abiding interest was with audio power amplifiers. He built many stereo amplifiers for friends and local recording studios. Many of these "one of a kind" components are still in use to this day.

Jeff's first "production" amplifiers and preamplifiers were built and sold in 1981, under the name of Rowland Research, and his small company debuted the Model 7 mono-block amplifier at the 1984 Consumer Electronics Show. Rowland Research became Jeff Rowland Design Group in 1987.

Since 1981, Jeff has developed more than 35 critically acclaimed components and pioneered many technologies now considered expected features of high end audio designs.

Jeff Rowland was the first to:

1. Introduce *symmetrically balanced high power amplification* to high end audio with the Model 7M monoblock amplifier in 1984.

2. Feature a full function infrared *remote control transmitter* unit and wired satellite receiver station on a reference preamplifier with the Consonance in 1989.
3. Refine and use *rechargeable battery DC power supplies* in reference grade amplifiers and preamplifiers.
4. Incorporate *Power Factor Correction (PFC)* into the design of high end power amplification with the Model 12 in 1998.
5. Incorporate extremely quiet, fully regulated, and blazingly nimble *switching mode power supplies (SMPS)* in truly high end stereo amplifiers, like the Model 10 stereo amplifier and the Model 12 monoblock power amplifier released in 1999.
6. Appy the ultra fast, ultra quiet and super low distortion *TI Burr Brown OPA1632* fully differential I/O audio amplifier modules in a high end audio product.
7. Utilize *transformer coupled input and output stages* into preamplifier design.

Thomas Holm, President, *Holm Acoustics*

For Thomas Holm, electronics is a life-long passion that started during his primary school years in Copenhagen, Denmark. By the 6th grade, he was soldering circuit boards for a course in basic electronics. Throughout high school, encouraged by his father's passion for music, Thomas experimented with his own design ideas by building custom audio speaker systems.

After high school, Thomas was determined to pursue his dreams. He enrolled in a one-year pre-college course of studies in electronics and mechanical design. This practical introduction to electronics was followed by a one year internship with Bruel & Kjaer, a company that developed laboratory equipment for audio and vibration measurements.

After his internship, Thomas returned to enrolled in a college degree program in Electrical Engineering. Thomas realized that the signaling processing and FFT techniques used at Bruel & Kjaer could be used in audio to control phase and amplitude simultaneously, and had the first inkling about products from his future company, Holm Acoustics. In partnership with Bruel & Kjaer, Thomas's graduation thesis involved the design of very high speed and high voltage Switch Mode Power Supplies (SMPS) that would modulate tunable lasers in new gas leak monitors.

Thomas completed his Bachelor degree in Electrical Engineering. His main focus was analog and digital design, signal processing, and medical equipment. He defended a thesis on capacitive sensors for audio speakers, where capacitive sensor-based servos monitored the movements of speaker membranes.

He soon realized that signal processing technology and FPGAs had major potential to evolve into mature technologies for audio products, as the DSPre ClockFlawless design, predecessor of the Aeris IsoSync ECS, later proved.

Thomas was hired by PhaseOne and tasked with transferring signal processing logic for high end digital camera sensors in FPGAs. Eventually he was developing CCD light sampling techniques, and designing entire cross A to D domain boards, 30dB more dynamic per pixel than commercial cameras.

The CCD light sampling techniques, dynamic optimization, and noise elimination logic that Thomas was developing for the professional market were incredibly innovative. The subsystems were so sensitive that they could measure single incoming light photons; in other words, they operated at a quantum level.

In 2000, Thomas was developing bi-phase H-bridge cardiac defibrillators. These newly designed defibrillators were smaller, more portable, and used significantly lower voltages than typical defibrillators. Thanks to several innovations introduced by Thomas Holmes, The products were much safer to use, and could be operated with little or no training.

In 2001, Thomas was back in the optical business, implementing FPGAs and cost optimizations for Contex, a company that specialized in very high speed large format scanners for professional applications. Taking advantage of FPGA signal processing logic, these devices operated at 40 to 80 MHz, and could process a one square meter document in as little as 10 seconds.

It became clear that FPGA-based processors had the capacity to perform the real-time mathematics required to implement audio components based on signal processing. The idea of creating DSPre 1 was now germinating.

By 2005, Mr. Holm had founded Holm Acoustics while doing part time consulting for optical digital systems, and continuing to develop the DSPre signal processing preamplifier, his first audio product released in 2008.

For more information on the Aeris DAC, please contact your nearest authorized Jeff Rowland Design Group dealer or distributor. A complete list of dealers and distributors is available on our website at http://jeffrowlandgroup.com.